UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/579,537	05/16/2006	Walter David Braddock	OSEMDB15UPCTUS	8472

31518 7590 03/05/2008
NEIFELD IP LAW, PC
4813-B EISENHOWER AVENUE
ALEXANDRIA, VA 22304

EXAMINER	
KIM, JAY C	

ART UNIT	PAPER NUMBER
2815	

NOTIFICATION DATE	DELIVERY MODE
03/05/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

general@neifeld.com
rneifeld@neifeld.com
rhahl@neifeld.com

Office Action Summary	Application No.	Applicant(s)	
	10/579,537	BRADDOCK, WALTER DAVID	
	Examiner	Art Unit	
	JAY C. KIM	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 71-91* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 71-91* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/7/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because abstract should be within the range of 50-150 words, but the abstract of current Application has more than 150 words. Correction is required. See MPEP § 608.01(b).

2. The disclosure is objected to because of the following informalities:

On line 10 of page 23, "a epitaxial" should be replaced by "an epitaxial".

On line 17 of page 24, "metal-oxide- -compound" should be replaced by "metal-oxide-compound".

Appropriate correction is required.

Claim Objections

3. Claims 71, 72, 76, 77 and 80 are objected to because of the following informalities:

On line 2 of claim 71, "one indium" should be replaced by "one of indium".

On line 2 of claim 72, "lease" should be replaced by "least".

On line 1 of claim 76, numeral 72 should be replaced by numeral 75, because a limitation of "gate electrode" is not recited in claim 1 or claim 72.

On line 1 of claim 77, numeral 72 should be replaced by numeral 75 or 76, because a limitation of "gate electrode" is not recited in claim 1 or claim 72.

On line 2 of claim 77, "group refractory gate metals" should be replaced by "group of refractory gate metals".

On line 1 of claim 80, "form" should be replaced by "formed".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 71-77 and 81-91 are rejected under 35 U.S.C. 103(a) as being unpatentable over Braddock (WO 02/15233) as modified by Hong et al. (US 6,469,357).

Regarding claim 1, Braddock discloses a metal-oxide-compound semiconductor field effect transistor structure (Fig. 1) comprising a compound semiconductor wafer structure (12) (line 7 of page 6) having an upper surface, a gate insulator structure (30) (line 15 of page 6) comprising a first layer (31) and a second layer (32), wherein the first layer (31) substantially comprises oxygen and gallium (lines 16-17 of page 6), the first layer (31) in contact with the upper surface, and wherein the second layer (32) comprises at least one insulating compound (lines 18-19 of page 6).

Braddock differs from the claimed invention by not comprising a nitride compound semiconductor wafer structure.

Hong et al. disclose a metal-oxide-compound semiconductor field effect transistor structure (Fig. 1) comprising a GaAs- or GaN-based semiconductor wafer structure (140) (col. 4, line 28 and col. 1, lines 24-26).

Since both Braddock and Hong et al. teach a metal-oxide-compound semiconductor field effect transistor structure, it would have been obvious to the one of ordinary skill in the art at the time the invention was made that the metal-oxide-compound semiconductor field effect transistor structure disclosed by Braddock may comprise a nitride compound semiconductor wafer structure disclosed by Hong et al., because forming a semiconductor field effect transistor structure using nitride-based semiconductors is well-known to improve device performance of a field effect transistor in applications such as microwave transmitters.

Regarding claims 71 and 72, Braddock further discloses that the at least one insulating compound comprises gallium and at least one rare earth element (lines 18-19 of page 6).

Regarding claims 73 and 74, Braddock further discloses for the structure of claim 1 that the at least one insulating compound comprises oxygen and at least one rare earth element (lines 18-19 of page 6).

Regarding claim 75, Braddock further comprises for the structure of claim 1 a gate electrode (17) (lines 21-22 of page 6) positioned on the gate insulator structure (30).

Regarding claim 76, Braddock further comprise source and drain regions (21 and 22) (line 24 of page 6 - line 1 of page 7) self-aligned to the gate electrode (17).

Regarding claim 77, Braddock further discloses that the gate electrode (17) comprises a metal selected from the group of refractory gate metals (lines 21-22 of page 6).

Regarding claim 81, Braddock further comprises for the structure of claim 1 a layer between the first layer (31) and the second layer (32) having a composition intermediate between the compositions of the first layer (31) and the second layer (32) (line 25 of page 4 - line 6 of page 5).

Regarding claim 82, Braddock further discloses for the structure of claim 1 that the first layer (31) has a thickness of more than 10 angstroms and less than 25 angstroms (lines 18-19 of page 4).

Regarding claim 83, Braddock further discloses for the structure of claim 1 that the gate insulator structure (30) has a thickness of 200-250 angstroms (lines 8-9 of page 8).

Regarding claims 84-86, Braddock in view of Hong et al. differ from the claimed invention by not showing that the upper surface comprises GaN (claim 84), $In_xGa_{1-x}N$ (claim 85) or $Al_xGa_{1-x}N$ (claim 86).

It would have been obvious to the one of ordinary skill in the art at the time the invention was made that the GaN-based semiconductor body (140) (col. 4, line 28 and col. 1, lines 24-26) disclosed by Hong et al. may comprise GaN, $In_xGa_{1-x}N$ or $Al_xGa_{1-x}N$, because GaN, $In_xGa_{1-x}N$ and $Al_xGa_{1-x}N$ are three well-known GaN-based semiconductors commonly used for forming a nitride-based semiconductor device including a field effect transistor, and it has been held to be within the general skill of a

worker in the art to select a known material on the basis of its suitability for the intended use. In re Leshin, 125 USPQ 416.

Regarding claim 87, Braddock discloses a field effect transistor (Fig. 1), which would comprise the structure of claim 1 in Braddock as modified by Hong et al.

Regarding claim 88, Braddock further discloses an integrated circuit (lines 4-9 of page 1), which would comprise the structure of claim 1 in Braddock as modified by Hong et al.

Regarding claim 89, Braddock discloses a method of making a metal-oxide-compound semiconductor field effect transistor structure (Fig. 1) comprising providing a compound semiconductor wafer structure (12) (line 7 of page 6) having an upper surface, providing a gate insulator structure (30) (line 15 of page 6) comprising a first layer (31) and a second layer (32), wherein the first layer (31) substantially comprises oxygen and gallium (lines 16-17 of page 6), the first layer (31) in contact with the upper surface, and wherein the second layer (32) comprises at least one insulating compound (lines 18-19 of page 6).

Braddock differs from the claimed invention by not comprising providing a nitride compound semiconductor wafer structure having an upper surface.

Hong et al. disclose a method of making a metal-oxide-compound semiconductor field effect transistor structure (Fig. 1) comprising providing a GaAs- or GaN-based semiconductor wafer structure (140) (col. 4, line 28 and col. 1, lines 24-26).

Since both Braddock and Hong et al. teach a method of making a metal-oxide-compound semiconductor field effect transistor structure, it would have been obvious to

the one of ordinary skill in the art at the time the invention was made that the method of making a metal-oxide-compound semiconductor field effect transistor structure disclosed by Braddock may comprise providing a nitride compound semiconductor wafer structure disclosed by Hong et al., because forming a semiconductor field effect transistor structure using nitride-based semiconductors is well-known to improve device performance of a field effect transistor in applications such as microwave transmitters.

Regarding claim 90, Braddock discloses a method of making a metal-oxide-compound semiconductor field effect transistor structure (Fig. 1) comprising providing a compound semiconductor wafer structure (12) (line 7 of page 6) having an upper surface, depositing a gate insulator structure (30) (line 15 of page 6) comprising depositing a first layer (31) and depositing a second layer (32), wherein the depositing the first layer (31) comprises depositing oxygen and gallium (lines 13-16 of page 7) onto the upper surface, and wherein depositing the second layer (32) comprises depositing at least one insulating compound (line 24 of page 7 - line 4 of page 8) onto the first layer (31).

Braddock differs from the claimed invention by not comprising providing a nitride compound semiconductor wafer structure having an upper surface.

Hong et al. disclose a method of making a metal-oxide-compound semiconductor field effect transistor structure (Fig. 1) comprising providing a GaAs- or GaN-based semiconductor wafer structure (140) (col. 4, line 28 and col. 1, lines 24-26).

Since both Braddock and Hong et al. teach a method of making a metal-oxide-compound semiconductor field effect transistor structure, it would have been obvious to

the one of ordinary skill in the art at the time the invention was made that the method of making a metal-oxide-compound semiconductor field effect transistor structure disclosed by Braddock may comprise providing a nitride compound semiconductor wafer structure disclosed by Hong et al., because forming a semiconductor field effect transistor structure using nitride-based semiconductors is well-known to improve device performance of a field effect transistor in applications such as microwave transmitters.

Regarding claim 91, Braddock discloses a method of using (lines 14-21 of page 10) a metal-oxide-compound semiconductor field effect transistor structure (Fig. 1), the structure (Fig. 1) comprising a compound semiconductor wafer structure (12) (line 7 of page 6) having an upper surface, a gate insulator structure (30) (line 15 of page 6) comprising a first layer (31) and a second layer (32), wherein the first layer (31) substantially comprises oxygen and gallium (lines 16-17 of page 6), the first layer (31) in contact with the upper surface, wherein the second layer (32) comprises at least one insulating compound (lines 18-19 of page 6).

Braddock differs from the claimed invention by not showing that the metal-oxide-compound semiconductor field effect transistor structure comprises a nitride compound semiconductor wafer structure, and that the method comprises applying a voltage to the gate insulator structure.

Hong et al. disclose a metal-oxide-compound semiconductor field effect transistor structure (Fig. 1) comprising a GaAs- or GaN-based semiconductor wafer structure (140) (col. 4, line 28 and col. 1, lines 24-26).

Since both Braddock and Hong et al. teach a metal-oxide-compound semiconductor field effect transistor structure, it would have been obvious to the one of ordinary skill in the art at the time the invention was made that the metal-oxide-compound semiconductor field effect transistor structure disclosed by Braddock may comprise a nitride compound semiconductor wafer structure disclosed by Hong et al., because forming a semiconductor field effect transistor structure using nitride-based semiconductors is well-known to improve device performance of a field effect transistor in applications such as microwave transmitters.

Further regarding claim 91, Braddock as modified by Hong et al. differ from the claimed invention by not showing the method of using the metal-oxide-compound semiconductor field effect transistor comprises applying a voltage to the gate insulator structure.

It would have been obvious, if not inherent, to the one of ordinary skill in the art at the time the invention was made that a voltage or a gate voltage can be applied to the gate insulator structure, because a gate voltage is commonly applied to a gate electrode and thus a gate insulator to operate a field effect transistor.

6. Claims 78-80 are rejected under 35 U.S.C. 103(a) as being unpatentable over Braddock (WO 02/15233) as modified by Hong et al. (US 6,469,357) in view of Hobson et al. (US 5,912,498). The teachings of Braddock as modified by Hong et al. are discussed above.

Regarding claims 78-80, Braddock as modified by Hong et al. differ from the claimed invention by not comprising a substrate (claim 78), wherein the nitride compound semiconductor wafer structure is built on the substrate (claim 79) and the substrate is formed from a member selected from the group consisting of sapphire, silicon, silicon on insulator, aluminum nitride, and gallium nitride (claim 80).

Hobson et al. disclose a metal-oxide-compound semiconductor field effect transistor structure (Fig. 4) comprising a substrate (40) (col. 4, lines 33-34), wherein a nitride compound semiconductor wafer structure (41) (col. 4, lines 33-35) is built on the substrate (40) and the substrate (40) is formed of sapphire (Al_2O_3).

Since both Braddock and Hobson et al. teach a metal-oxide-compound semiconductor field effect transistor structure, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the metal-oxide-compound semiconductor field effect transistor structure disclosed by Braddock as modified by Hong et al. with the sapphire substrate for a GaN wafer structure disclosed by Hobson et al., because a sapphire substrate is commonly used for forming a GaN wafer structure due to its low cost.

Double Patenting

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140

F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. Claims 1, 71-77, 82-91 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 7, 8, 11 and 18-20 of U.S. Patent No. 6,989,556. Although the conflicting claims are not identical, they are not patentably distinct from each other because when the upper surface of the compound semiconductor wafer structure recited in claim 1 of US 6,989,556 comprises GaN, InGaN or AlGaN as recited in claims 18-20 of US 6,989,556, the compound semiconductor wafer structure has a nitride compound semiconductor wafer structure recited in claim 1 of current Application.

9. Claims 1, 71-77, 82-91 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 7, 8, 11, 18-20 and 23 of U.S. Patent No. 7,187,045. Although the conflicting claims are not identical, they are not patentably distinct from each other because when the upper surface of the compound semiconductor wafer structure recited in claim 1 of US 7,187,045 comprises GaN, InGaN or AlGaN as recited in claims 18-20 of US 7,187,045, the compound

semiconductor wafer structure has a nitride compound semiconductor wafer structure recited in claim 1 of current Application.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAY C. KIM whose telephone number is (571)270-1620. The examiner can normally be reached on 7:30 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Matthew C. Landau/
Primary Examiner, Art Unit 2815

/J. K./
Examiner, Art Unit 2815
February 20, 2008